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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,307	12/31/2003	Mohamed Soufi	03226/356001; SUN040029	8806

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EXAMINER	
OCHOA, JUAN CARLOS	

ART UNIT	PAPER NUMBER
2123	

NOTIFICATION DATE	DELIVERY MODE
10/24/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/751,307	SOUFI ET AL.	
	Examiner	Art Unit	
	Juan C. Ochoa	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-12 and 14-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-12 and 14-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed 8/20/07 has been received and considered. Claims 1–5, 7–12, and 14–22 are presented for examination.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/20/07 has been entered.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1–5, 7–12, and 14–20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ping-Sheng Tseng, (Tseng (2) hereinafter), U.S. Patent 6,785,873 taken in view of Eisenhofer et al., (Eisenhofer hereinafter), U.S. Patent 6,108,494.

7. As to claim 1, Tseng (2) discloses a method for providing verification for a simulation image (see col. 14, lines 45–58), comprising: producing an optimized image (see col. 22, lines 9–11); removing nodes from the simulation image to produce an optimized image and an optimized nodes image (see col. 26, lines 62–65); when debugging is selected, simulating the reconstructed simulation image to gather simulation data (see col. 45, lines 13–29), wherein the reconstructed simulation image comprises the optimized image and the optimized nodes image; debugging the simulation image using simulation data (see col. 46, lines 17–28); and verifying one

selected from a group consisting of the optimized image and the reconstructed simulation image (see col. 48, lines 25–36).

8. While Tseng (2) discloses removing nodes from the simulation image to produce an optimized image and an optimized nodes image, Tseng (2) fails to expressly disclose an optimized nodes image comprising information about the nodes removed from the simulation image.

9. Eisenhofer discloses an optimized nodes image comprising information about the nodes removed from the simulation image (see "boundary nets database" in col. 8, lines 11–16).

10. Tseng (2) and Eisenhofer are analogous art because they are both related to verification of electronic systems.

11. Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to utilize the teachings of Eisenhofer in the method of Tseng (2) because Eisenhofer provides netlist optimization logic that analyzes netlists associated with partitions of a design that have been allocated to a plurality of solvers (see col. 3, lines 59–61), and as a result, Eisenhofer reports the following improvement over his prior art: optimized boundary net information and/or netlist information which may subsequently be used to reduce runtime synchronization during a simulation session (see col. 3, lines 62–65).

12. As to claim 2, Tseng (2) discloses a method wherein the simulation image and the reconstructed simulation image comprise a register transfer level design (see col. 26, lines 49–50).

13. As to claim 3, Tseng (2) discloses a method wherein debugging comprises comparing a reference value to a value of a corresponding register transfer level design component of at least one selected from the group consisting of the optimized image and the reconstructed simulation image (see col. 46, lines 3–16).

14. As to claim 4, Tseng (2) discloses a method wherein the optimized nodes image comprises at least one node selected from the group consisting of a redundant node, an unobservable node, and a dangling node (see "redundant and unused" in col. 26, lines 62–65).

15. As to claim 5, Eisenhofer discloses a method wherein the optimized nodes image comprises a list of optimized nodes (see "list of boundary nets" in col. 8, lines 11–13) and information about how to compute the optimized nodes image from the optimized image (see col. 8, lines 53–59).

16. As to claim 7, Tseng (2) discloses a method further comprising: isolating and eliminating a bug in the simulation image using simulation data (see col. 44, lines 31–32).

17. As to claims 8–12 and 14, these claims recite a computer system for performing the method of claims 1–5 and 7. Tseng (2) discloses a system (see col. 4, lines 1–2) for performing a method that teaches claims 1–5 and 7. Therefore, claims 8–12 and 14 are rejected for the same reasons given above.

18. As to claim 15, Tseng (2) discloses a system (see col. 4, lines 1–2) for verifying a simulation image (see col. 14, lines 45–58), comprising: an optimizer tool providing functionality to remove nodes from the reconstructed simulation image to produce an

optimized image and an optimized nodes image (see col. 26, lines 62–65); a test vector providing an input signal value for a component in at least one selected from the group consisting of the optimized image and a reconstructed simulation image (see "test vector" as "simulation history file" in col. 45, lines 13–31); a reconstructor tool of a testbench providing functionality to provide the reconstructed simulation image using the optimized image and the optimized nodes image (see col. 45, lines 1–6), when debugging is selected (see col. 45, lines 16–18), wherein the testbench provides functionality to: simulate the reconstructed simulation image to gather simulation data, debug simulation image using simulation data, and verify at least one selected from the group consisting of the optimized image and the reconstructed simulation image using the test vector (see col. 45, lines 18–29). While Tseng (2) discloses an optimizer tool providing functionality to remove nodes from the reconstructed simulation image to produce an optimized image and an optimized nodes image, Tseng (2) system lacks an optimized nodes image comprising information about the nodes removed from the simulation image. Eisenhofer discloses an optimized nodes image comprising information about the nodes removed from the simulation image (see "boundary nets database" in col. 8, lines 11–16).

19. As to claims 16–20, these claims recite a computer system for performing the method of claims 1–5. Tseng (2) discloses a system (see col. 4, lines 1–2) for performing a method that teaches claims 1–5. Therefore, claims 16–20 are rejected for the same reasons given above.

20. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng (2) taken in view of Eisenhofer, and further in view of Moriguchi et al., (Moriguchi hereinafter), U.S. Patent 6,088,821.

21. As to claim 21, while the Tseng (2)–Eisenhofer method removes nodes from the simulation image to produce an optimized image and an optimized nodes image, the Tseng (2)–Eisenhofer method fails to disclose removing nodes from the simulation image further comprising moving at least one sequential element to use an input of the optimized nodes image as an output of the optimized nodes image.

22. Moriguchi discloses a method wherein removing nodes from the simulation image further comprises moving at least one sequential element to use an input of the optimized nodes image as an output of the optimized nodes image. (See col. 3, lines 14–19; col. 9, line 64 to col. 10, line 8; and Fig. 10).

23. Tseng (2), Eisenhofer, and Moriguchi are analogous art because they are related to verification of electronic systems.

24. Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to utilize the teachings of Moriguchi in the Tseng (2)–Eisenhofer method because Moriguchi provides high speed logic circuit verification (see col. 1, line 66 to col. 2, line 4), and as a result, Moriguchi reports the following improvement over his prior art: reducing the number of times of event changes occurring in simulation by excluding flip-flops which do not influence logic, i.e. deleting redundant flip-flops, and rearranging combinational circuits (see col. 11 lines 1–8, 12–19, and 27–32).

25. As to claim 22, Moriguchi discloses a method wherein the software instructions to remove nodes from the simulation image further comprise software instructions to move at least one sequential element to use an input of the optimized nodes image as an output of the optimized nodes image producing the optimized image. (See col. 3, lines 14–19; col. 9, line 64 to col. 10, line 8; and Fig. 10).

Response to Arguments

26. Applicant's arguments filed 8/20/07 have been fully considered and they are persuasive.

27. Regarding the rejection under 103. Applicant's arguments with respect to claims 1–5, 7–12, and 14–22 have been considered but are moot in view of the new ground(s) of rejection. In the instant rejection, Examiner has elaborated prior art disclosures of amended claims.

Conclusion

28. Examiner would like to point out that any reference to specific figures, columns and lines should not be considered limiting in any way, the entire reference is considered to provide disclosure relating to the claimed invention.

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan C. Ochoa whose telephone number is (571) 272-2625. The examiner can normally be reached on 7:30AM - 4:00 PM.

30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

31. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

*** 9/30/07 JO

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